FORM PTO-1390 (REV 5-93)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY DOCKET NO. 107400-00045
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		DATE: January 14, 2002
		U.S. APPLN. NO. (IF KNOWN, SEE 37 C.F.R. 1.5) Not Yet Assigned 10/030089
INTERNATIONAL APPLICATION NO. PCT/JP00/04715	INTERNATIONAL FILING DATE 13 July 2000	PRIORITY DATE CLAIMED 15 July 1999

TITLE OF INVENTION: SEMICONDUCTOR DEVICE HAVING MOS FIELD-EFFECT TRANSISTOR

APPLICANT(S) FOR DO/EO/US: Kazuhisa SAKAMOTO

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371. (THE BASIC FILING FEE IS ATTACHED)

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This express request to begin national examination procedures [35 U.S.C. 371(f)] at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☐ A proper demand for International Preliminary Amendment was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed [35 U.S.C. 371(c)(2)]
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).

6. ☐ A translation of the International Application into English [35 U.S.C. 371(c)(2)].

7. ☒ Amendments to the claims of the International Application under PCT Article 19 [35 U.S.C. 371(c)(3)]
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 [35 U.S.C. 371(c)(3)].

9. ☒ An oath or declaration of the inventor(s) [35 U.S.C. 371(c)(4)].

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 [35 U.S.C. 371(c)(5)].

Items 11 - 16 below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.

13. ☐ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☒ Other items or information: ☒ Cover sheet of published International Application WO 01/06569
    Drawings (3 sheets)

U.S. APPLN. NO. (IF KNOWN SEE 37 C.F.R. 1.5) 10/030089	INTERNATIONAL APPLICATION NO. PCT/JP00/04715	ATTORNEY DOCKET NO. 107400-00045 DATE: January 14, 2002

17. ☒ The following fees are submitted:	CALCULATIONS / PTO USE ONLY
Basic National Fee [37 C.F.R. 1.492(a)(1)-(5)]:	
Search Report has been prepared by the EPO or JPO.....$890.00	
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482).....$710.00	
No international preliminary examination fee paid to USPTO (37 C.F.R. 1.482) but international search fee paid to USPTO [37 C.F.R. 1.445(a)(2)].....$740.00	
Neither international preliminary examination fee (37 C.F.R. 1.482) or international search fee [37 C.F.R. 1.445(a)(2)] paid to USPTO.....$1,040.00	
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4).....$ 100.00	

ENTER APPROPRIATE BASIC FEE AMOUNT =				$ 890.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date [37 C.F.R. 1.492(e)].				$ 0.00	
Claims	Number Filed	Number Extra	Rate		
Total Claims	6 - 20 =	0	X $ 18.00	$ 0.00	
Independent Claims	1 - 3 =	0	X $ 84.00	$ 0.00	
Multiple dependent claim(s) (if applicable)			+ $280.00	$ 0.00	
TOTAL OF ABOVE CALCULATIONS =				$ 890.00	
Reduction by one-half for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 C.F.R. 1.9, 1.27, 1.28).				$ 0.00	
SUBTOTAL =				$ 890.00	
Processing fee of $130.00 for furnishing the English translation later the ☐ 20 ☐ 30 months from the earliest claimed priority date [37 C.F.R. 1.492(f)]. +				$ 0.00	
TOTAL NATIONAL FEE =				$ 890.00	
Fee for recording the enclosed assignment [37 C.F.R. 1.21(h)]. The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). $40.00 per property +				$ 40.00	
TOTAL FEES ENCLOSED =				$ 930.00	
				Amount to be refunded	$
				Charged	$

a. ☒ A check in the amount of $930.00 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. 01-2300 in the amount of $ to cover the above fee. A duplicate copy of this sheet is enclosed.
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 01-2300.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive [37 C.F.R. 1.137(a) or (b)] must be filed and granted to restore the application to pending status.

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10/030089
531 Rec'd PCT/PTO 14 JAN 2002

3/PRTS

S P E C I F I C A T I O N

BE IT KNOWN THAT I, KAZUHISA SAKAMOTO, residing at c/o ROHM CO., LTD., 21, Saiin Mizosaki-cho, Ukyo-ku, Kyoto-shi, Japan, subjects of Japan, have invented certain new and useful improvements in

SEMICONDUCTOR DEVICE HAVING MOS FIELD-EFFECT TRANSISTOR

of which the following is a specification:-

SPECIFICATION

SEMICONDUCTOR DEVICE HAVING MOS FIELD-EFFECT TRANSISTOR

FIELD OF THE INVENTION

[0001] The present invention relates to a semiconductor device having a MOS field-effect transistor (hereinafter abbreviated as MOSFET) such as a vertical-type power MOSFET or a double diffusion-type MOSFET. More particularly, the present invention relates to such a MOSFET that has a very short turn-ON/OFF time and an improved reverse withstanding voltage.

BACKGROUND ART

[0002] A driver circuit is frequently used which employs a vertical-type or double diffusion-type power MOSFET to drive an inductive load such as a motor. For example, the vertical-type power MOSFET has such a configuration, as shown in FIG. 4, that a P-well 21 is formed on the surface of an N-type semiconductor layer 20 provided on a N^+-type semiconductor substrate 20a, and at an outer periphery of this P-well 21 is formed a ring-shaped N^+-type source diffusion layer 22. In this configuration, the semiconductor layer 20 outside the P-well 21 and the semiconductor substrate 20a act as a drain layer 23.

[0003] The surface region of the P-well 21 between the drain layer 23 and the source layer 22 acts as a channel

region 26, on which is provided a gate electrode 28 with a gate insulator film 27 interposed therebetween. At the center of the P-well 21 is provided a P^+-type region 25 for ohmic-contact such that a source electrode 33 may be connected to this P^+-type region 25 and the source region 22. The drain electrode 24 is provided on the back surface of the semiconductor substrate 20a. Thus, the vertical-type MOSFET is formed.

[0004] A PN junction of the P-well 21 and the N-type semiconductor layer 20 forms a so-called built-in diode (body diode). This built-in diode is structured so as to be connected in the reverse direction between the drain and the source and can be used as a flywheel diode for inducing a reverse recovery current ascribed to a counter electromotive force of an inductive load.

[0005] The counter electromotive force of the inductive load acts to apply a voltage in the forward direction on the built-in diode, which is accompanied, as well known, by accumulation of minority carrier, that is, electrons in the P-well. Thus accumulated minority carrier inhibits rapid interruption of the operation of the built-in diode at the time of rectification when the current is changed in flow direction. Moreover, if the flow of this minority carrier is concentrated to part of the device, the PN junction portion of the P-well and the drain layer is broken and hence the power MOSFET is broken eventually.

[0006] In view of the above, it is an object of the invention

to provide a semiconductor device including a MOSFET that can solve these technological problems in providing high-speed switching operations of a built-in diode and improving the breakdown resistance amount (withstanding voltage).

DISCLOSURE OF THE INVENTION

[0007] A semiconductor device including a MOS field-effect transistor according to the present invention includes; a MOS field-effect transistor; and a diode which is built in the transistor and connected between a source electrode and a drain electrode thereof so that when a voltage in the reverse direction is applied between the source electrode and the drain electrode at the time of operation, which forms a current path between the source electrode and the drain electrode, wherein a contact portion of the diode with the source electrode has such a construction that a high-impurity concentration region having a second conductivity type which is a conductivity type of the source electrode side semiconductor layer of the diode, and a region having a first conductivity type opposite to the conductivity type or a low-impurity concentration region having the second conductivity type are formed alternately in a plan structure.

[0008] The "high-impurity concentration" of the high-impurity concentration region of the second conductivity type means such an impurity concentration as to form an ohmic

contact with the source electrode.

[0009] By this construction, if a counter electromotive force is generated when an inductive load such as a motor connected to a circuit having a device of the present invention is turned OFF, a resultant voltage in the reverse direction applied between the drain and the source is cancelled by the built-in diode, after which the minority carrier remaining in the second conductivity type region is dropped into the first conductivity type region of the contact portion, thus enabling suppressing the accumulation of the minority carrier in the second conductivity type region. This mechanism enables rapidly not to make a working of the built-in diode. Also, since the minority carrier is not accumulated, a large current is not concentrated to part of the device at the time of rectification, thus enabling enhancing the withstanding voltage.

[0010] Specifically, this effect is remarkable especially when the MOS field-effect transistor is a double-diffusion type MOS field-effect transistor that has a first conductivity type semiconductor layer which provides a drain region, second conductivity type regions which are formed by diffusion in the first conductivity type semiconductor layer, and source regions having a first conductivity type formed by diffusion at an outer periphery of each of the second conductivity type regions in such a configuration that such portions of the second conductivity type regions which are positioned between each of the source regions and

the drain region act as channel regions.

[0011] More specifically, the source electrode is provided so as to be in contact with each of the source regions and a surface portion of each of the second conductivity type regions opposite to each of the channel regions with respect to each of the source regions. Further, the second conductivity type regions are formed in a matrix in the first conductivity type semiconductor layer, each of the source regions is formed in a ring shape on a plan view in each of the second conductivity type regions so as to give a constant gap at the periphery of each of the second conductivity type regions, and also the source electrode is formed at a predetermined region of an inner circumference of each of the ring-shaped source regions and the entire inner surface of each of the second conductivity type regions, thus providing a mass-capacity power MOSFET.

[0012] Specifically, the contact portion has such a construction that a contact portion of each of the second conductivity type regions with the source electrode has such a construction that one or more first conductivity type high impurity-concentration regions each of which is ring shape on a plan view and one or more second conductivity type high impurity-concentration regions are provided alternately or that the second conductivity type regions have a low impurity concentration; and wherein a contact portion of each of the second conductivity type regions with the source electrode has such a construction that second conductivity type high

impurity-concentration regions are evenly spaced in each of the second conductivity type regions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 is an expanded perspective and partial cross-sectional view for showing a construction of a MOSFET according to one embodiment of the present invention;

[0014] FIGS. 2A and 2B are a plan view and a cross-sectional view respectively, for showing a construction of a contact portion with a source electrode which is removed;

[0015] FIG. 3 is a cross-sectional view for showing another example of the construction of the contact portion; and

[0016] FIG. 4 is a cross-sectional view for showing an example of a construction of a prior art vertical-type MOSFET.

BEST MODE FOR CARRYING OUT THE INVENTION

[0017] The following will describe a semiconductor device having a MOSFET according to the present invention with reference to the drawings. As can be seen from its cross-sectional view of one embodiment shown in FIG. 1, in a semiconductor device having a MOSFET of the present invention, in a surface of the N-type semiconductor layer 20 is formed a predetermined pattern of a P-wells 21 by diffusion. For example, directly below a gate pad 36 to which a gate terminal 35 is connected, a large-area P-well 21a (P-well below the pad) is formed, and in the remaining region

is formed an evenly spaced plurality of the P-wells 21 in a matrix pattern, and each of P-wells 21 is, for example, rectangular in a plan view.

[0018] At the outer periphery of each of the P-wells 21 is formed, for example, a rectangular ring-shaped N^+-type diffused source region 22. The semiconductor layer 20 except this P-well 21 and an N^+-type semiconductor substrate 20a on which this semiconductor layer 20 is grown act as a drain region 23, thus providing a vertical-type double-diffusion MOSFET. On the back side surface of the N^+-type semiconductor substrate 20a is provided a drain electrode 24.

[0019] In the P-well 21, a surface layer portion positioned between the drain region 23 and the diffused source region 22 provides a channel region 26 in which is formed a channel 50 when the MOSFET is turned ON. Above this channel region 26 is formed a gate electrode 28 with a gate insulator film 27 interposed therebetween. The gate electrode 28 directly below the gate pad 36 is connected to the gate pad 36 through a contact hole 30 formed in the insulator film 29 on the gate electrode 28. The other gate electrodes 28 are connected to the gate electrodes 28 directly below the gate pad 36 at a position not shown in the figure.

[0020] In the insulator film 29 are formed, on the surface of each P-well 21, a source contact hole 31 for exposing the diffused source region 22 provided in this P-well 21 and the surface of the P-well 21 surrounded by this diffused source

region 22. A source electrode 33 formed on the insulator film 29 is commonly connected through this source contact holes 31 to all of the diffused source region 22 provided on the surface of each P-well 21 and the surfaces of portions surrounded by the diffused source region 22 in each P-well 21.

[0021] This results in such a construction that between the source electrode 33 and the drain electrode 24 is connected a diode consisting of a PN junction of the P-well 21 and the N-type semiconductor layer 20 (drain region), which diode acts as a built-in diode D that becomes conductive when a voltage in the reverse direction to that applied when this MOSFET is operated is applied across itself. That is, this built-in diode D may be used as a flywheel diode for flowing therethrough a reverse recovery current ascribed to a reverse electromotive force of an inductive load such as a motor when this MOSFET is used to drive it.

[0022] The invention features that a contact portion 40 of the p-well 21 with the source electrode 33 is not formed of a contact region only of a p^+-type region but is formed in such a configuration that a P^+-type region and an N^+-type region alternate with each other in a plan view.

[0023] That is, as shown in FIG. 2A illustrating a plan view of the contact portion 40 with the source electrode 33 etc. as removed and FIG. 2B illustrating an expanded cross-sectional view of part of FIG. 2A, in the outer surface

layer of such a region of the P-well 21 that is surrounded by the rectangular ring-shaped diffused source region 22 are formed concentrically a small-width N^+-type (or N-type) ring-shaped region 41 and an equivalently small-width P^+-type ring-shaped region 42 alternately. These regions 41 and 42 make up the contact portion 40 and all come in contact with the source electrode 33 in an ohmic manner. That is, the N^+-type region 41 and the P^+-type region 42 are arrayed alternately in a plan view.

[0024] In such a configuration, electrons, if any as a minority carrier in the P-well 21, fall in the N^+-type region 41 and then can be drawn out to the source electrode 33 rapidly. Thus, it is possible to suppress the accumulation of electrons in the P-well 21.

[0025] When the MOSFET according to this embodiment is used to drive an inductive load such as a motor, a turn-ON voltage is applied at the gate electrode 28 to form a channel 50 (see FIG. 1) to thereby interconnect the source region 22 and the drain region 23 therethrough. When the MOSFET is ON, it turns out as a voltage in the reverse direction is applied on the built-in diode D, which results in as the built-in diode D presents no actions.

[0026] When a turn-OFF voltage is applied at the gate to give a non-conductive state between the source and drain regions, a reverse electromotive force is applied from the inductive load to apply a voltage in the forward direction to the built-in diode D, through which in turn a reverse

recovery current flows, thus canceling the reverse electromotive force. In this case, a minority carrier (electrons in an example shown in FIG. 1), if left in the P-well 21, may retard the operations of the transistor when a turn-ON voltage is applied on its gate and so needs to disappear rapidly. For this purpose, by the invention, the contact portion of the diode D with the source electrode has such a construction that the N^+-type and P^+-type regions alternate with each other in the P-well, so that the minority-carrier electrons can fall into the N^+-type region and then be drawn out to the source electrode.

[0027] Thus, a current can flow immediately when the MOSFET is turned ON, so that at the time of commutation (when such a situation occurs that a voltage in the reverse direction is applied to the built-in diode), the built-in diode D can be immediately blocked (turned OFF), thus shortening the reverse recovery time (t_{rr}) significantly. Besides, no electrons are accumulated in the P-well 21, so that no large current is concentrated during commutation nor is destroyed the PN junction of the built-in diode D. These features enable manufacturing such a MOSFET that has significantly improved breakdown resistance amount as compared to that of the prior art construction.

[0028] Specifically, the reverse recovery time t_{rr} of the built-in diode D could be shortened by about 30% and the avalanche current (largest current that does not destroy the PN junction) of the built-in diode D could be increased by

about 20%.

[0029] FIG. 3 is a cross-sectional view for showing another configuration example of the contact portion 40 between the P-well and the source electrode 33. In FIG. 3, the same elements as those in FIGS. 1, 2A and 2B are indicated by the same reference numerals. In this example, the contact portion 40 is comprised of a plurality of evenly spaced P^+-type regions 42. Therefore, in the construction shown by the cross-sectional view of FIG. 3 or a construction of a plan view not shown (similar to FIG. 2A), the P^+-type region 42 and the P-well 21 region are formed alternately. This P-well 21 has a low impurity concentration and has a Schottky junction formed between itself and the source electrode 33.

[0030] In this construction, the minority-carrier electrons in the P-well 21 are rapidly released through the Schottky junction portion with the source electrode 33. That is, the Schottky portion has the same actions as those by the N^+-type region shown in FIGS. 2A and 2B to thereby rapidly remove the minority-carrier electrons, thus achieving the same effects as those mentioned above.

[0031] The N^+-type region 41 may be an N-type region as far as an ohmic contact can be obtained with the source electrode 33 in terms of impurity concentration and also, the contact portion 40 of the P-well 21 with the source electrode 33 having a configuration that one pair of a P^+-type region and an N^+-type (or N-type) region or P-type region are formed functions as a minority-carrier take-in

structure of the invention.

[0032] Although one embodiment of the invention has been described, the invention is applicable also to other embodiments. For example, although the above-mentioned embodiment has employed a vertical-type double-diffusion MOSFET, the present invention is applicable also to a horizontal-type double-diffusion MOSFET and not limited to double-diffusion MOSFET even also to a CMOSFET with the same construction. Further, although an N-channel type MOSFET has been exemplified, the invention is applicable also to a P-channel type MOSFET. In this case, for example, an N^+ region and a P^+ region may be arrayed alternately in an N-well or a plurality of N^- regions is evenly spaced to provide a Schottky junction portion. In the Schottky junction portion in such a case, some of the electrode materials for the source electrode 33 may be made of Titanium (Ti) or Molybdenum (Mo) in place of Aluminum (Al).

[0033] Also, the impurity-diffused regions which make up the contact portion need not be formed concentrically but may be formed in a straight stripe or any other appropriate shape. For example, when the P-well is formed in a stripe shape and source regions are also formed in a stripe shape therein, preferably the contact portion is formed in a stripe shape correspondingly.

[0034] Further, although the above-mentioned embodiment has exemplified such a semiconductor device that has one MOSFET, the invention is applicable also to such a

semiconductor device that has a plurality of MOSFETs or that a functional element other than a MOSFET on the same semiconductor substrate.

INDUSTRIAL APPLICATION

[0035] By the present invention, it is possible to obtain a MOSFET which has a fast switching speed and a high breakdown resistance amount (withstanding voltage) and effectively use it in, for example, a power source IC, a motor driver, or a solenoid drive in a DVD apparatus, a portable audio apparatus, a switching power source, and the like.

What is claimed is:

1. A semiconductor device comprising:

a MOS field-effect transistor; and

a diode which is built in said transistor and connected between a source electrode and a drain electrode thereof so that when a voltage in the reverse direction is applied between said source electrode and said drain electrode at the time of operation , which forms a current path between said source electrode and drain electrode,

wherein a contact portion of said diode with said source electrode has such a construction that a high-impurity concentration region having a second conductivity type which is a conductivity type of said source electrode side semiconductor layer of said diode, and a region having a first conductivity type opposite to said conductivity type or a low-impurity concentration region having said second conductivity type are formed alternately in a plan structure.

2. The semiconductor device of claim 1, wherein said MOS field-effect transistor is a double-diffusion type MOS field-effect transistor that has a first conductivity type semiconductor layer which provides a drain region, second conductivity type regions which are formed by diffusion in said first conductivity type semiconductor layer, and source regions having a first conductivity type formed by diffusion at an outer periphery of each of said second conductivity type regions in such a configuration that such portions of

said second conductivity type regions which are positioned between each of said source regions and said drain region act as channel regions.

3. The semiconductor device of claim 2, wherein said source electrode is provided so as to be in contact with each of said source regions and a surface portion of each of said second conductivity type regions opposite to each of said channel regions with respect to each of said source regions.

4. The semiconductor device of claim 3, wherein said second conductivity type regions are formed in a matrix in said first conductivity type semiconductor layer, each of said source regions is formed in a ring shape on a plan view in each of said second conductivity type regions so as to give a constant gap at the periphery of each of said second conductivity type regions, and also said source electrode is formed at a predetermined region of an inner circumference of each of said ring-shaped source regions and the entire inner surface of each of said second conductivity type regions.

5. The semiconductor device of claim 4, wherein a contact portion of each of said second conductivity type regions with said source electrode has such a construction that one or more first conductivity type high impurity-concentration regions, each of which is ring shape on a plan view and one or more second conductivity type high impurity-concentration regions are provided alternately.

6. The semiconductor device of claim 4, wherein each

of said second conductivity type regions has a low impurity concentration; and wherein a contact portion of each of said second conductivity type regions with said source electrode has such a construction that second conductivity type high impurity-concentration regions are evenly spaced in each of said second conductivity type regions.

FIG. 1

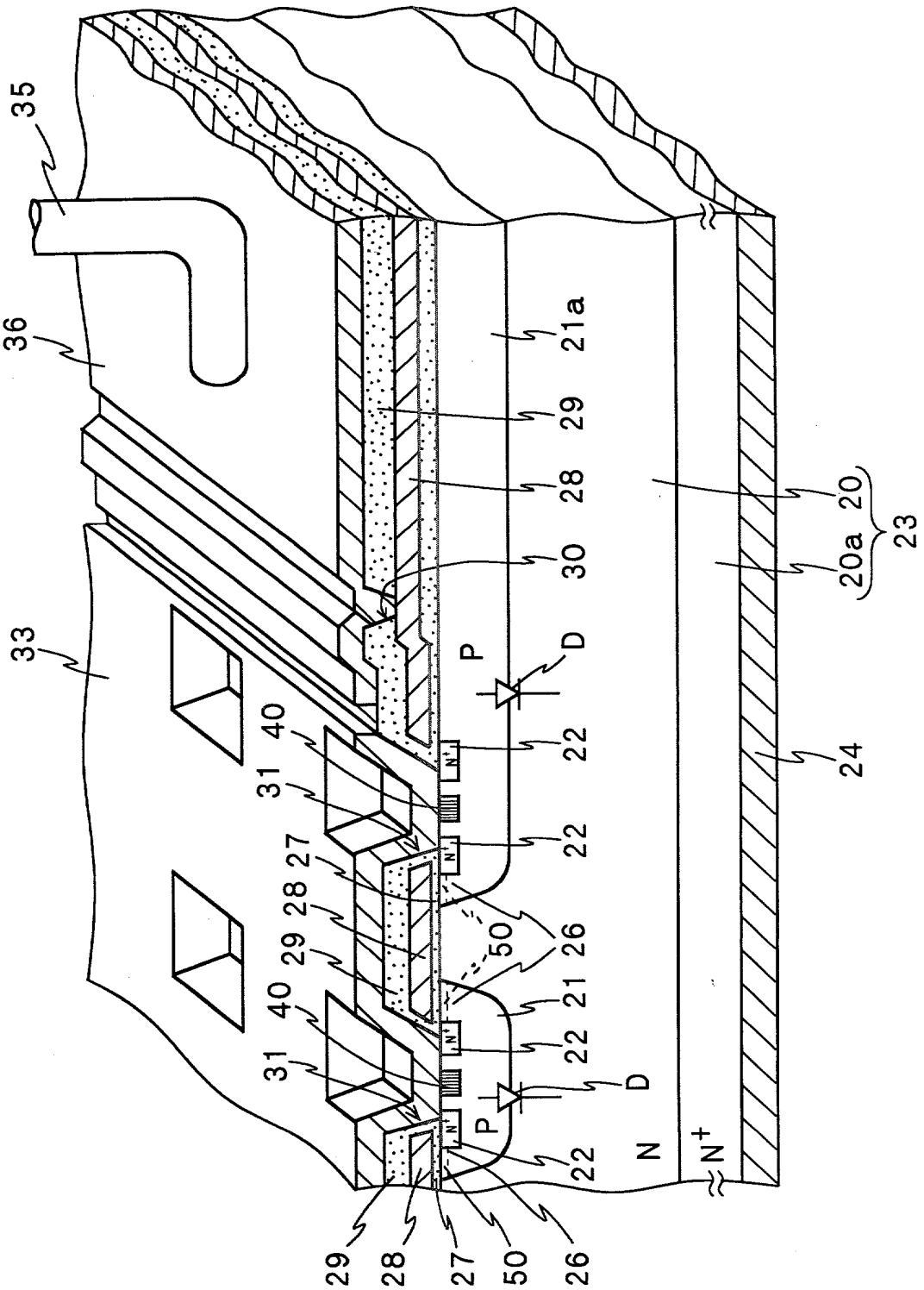

FIG. 2A

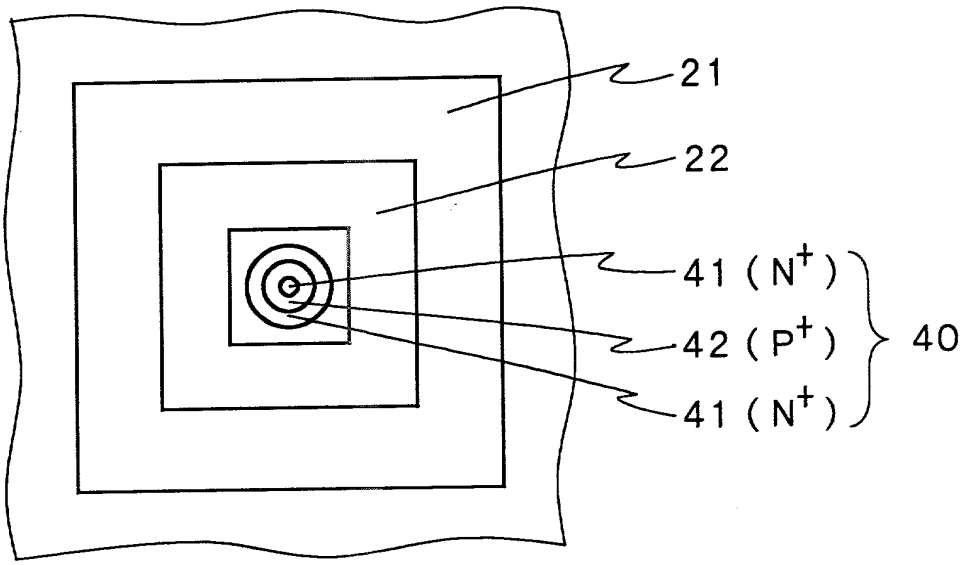

FIG. 2B

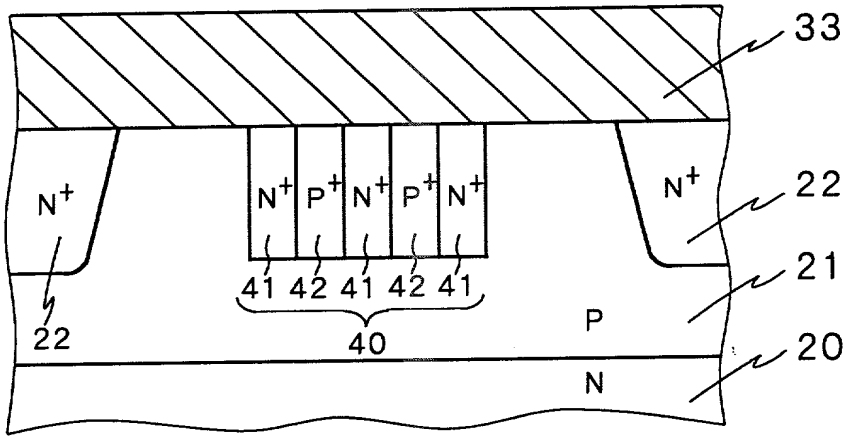

FIG. 3

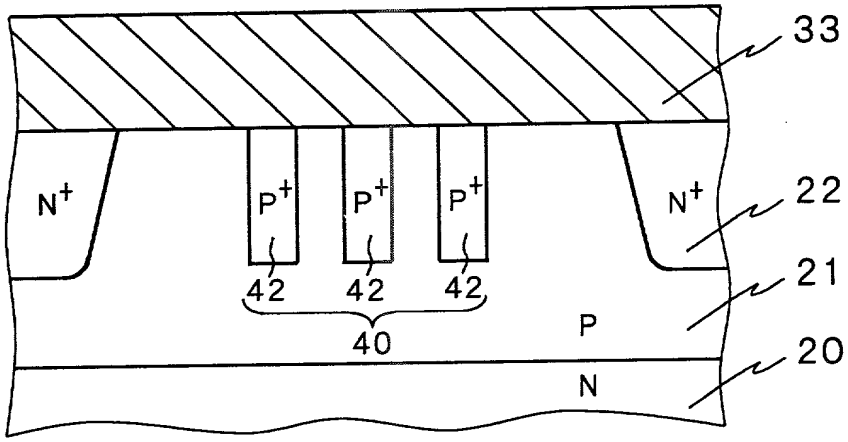
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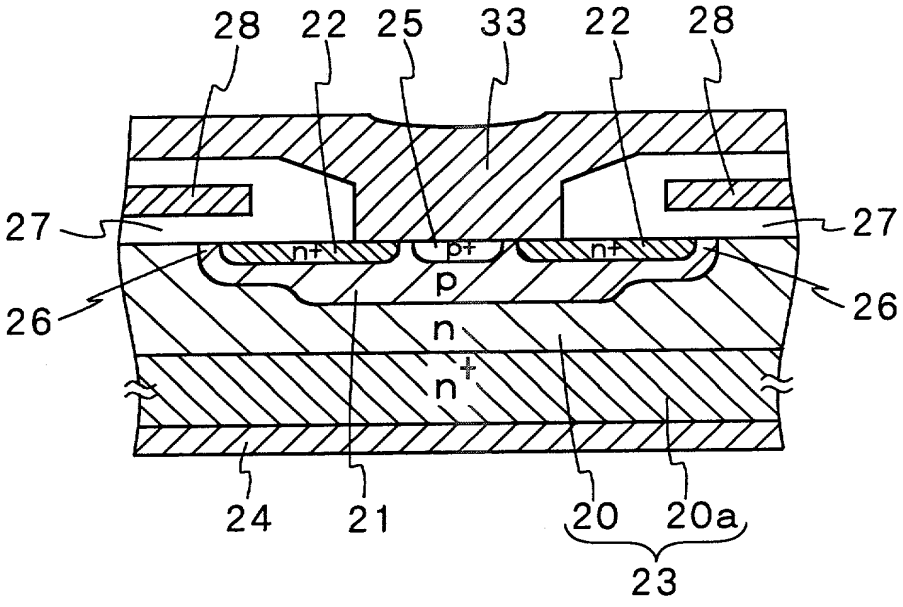
FIG. 4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PTO/SB/106 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE HAVING

MOS FIELD-EFFECT TRANSISTOR

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____ に訂正されました。

☒ was filed on July 13, 2000
as United States Application Number or
PCT International Application Number
PCT/JP00/04715 and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条(a)-(d)項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約３６５(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
H11-201875	Japan	15/07/1999	☐
			☐

私は、第３５編米国法典１１９条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣言を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

書類送付先

(13)

And I hereby appoint as principal attorneys: David T. Nikaido, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. 25,895; George E. Oram, Jr., Reg. No. 27,931; Robert B. Murray, Reg. No. 22,980; Martin S. Postman, Reg. No. 18,570; E. Marcie Emas, Reg. No. 32,131; Douglas H. Goldhush, Reg. No. 33,125; Kevin C. Brown, Reg. No. 32,402; Monica Chin Kitts, Reg. No. 36,105; Richard J. Berman, Reg. No. 39,107; King L. Wong, Reg. No. 37,500; Karen K. Costantino, Reg. No. 35,107; and James A. Poulos, III, Reg. No. 31,714.

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発明者の署名 日付	Inventor's signature Date Kazuhisa Sakamoto 27/12/2001
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第二共同発明者名	Full name of second joint inventor, if any
第二共同発明者の署名 日付	Second inventor's signature Date
住所	Residence
国籍	Citizenship
私書箱	Post Office Address

（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

第三共同発明者名		Full name of third joint inventor, if any	
第三共同発明者の署名	日付	Third inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第四共同発明者名		Full name of fourth joint inventor, if any	
第四共同発明者の署名	日付	Fourth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第五共同発明者名		Full name of fifth joint inventor, if any	
第五共同発明者の署名	日付	Fifth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第六共同発明者名		Full name of sixth joint inventor, if any	
第六共同発明者の署名	日付	Sixth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	

第七共同発明者名		Full name of seventh joint inventor, if any	
第七共同発明者の署名	日付	Seventh inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第八共同発明者名		Full name of eighth joint inventor, if any	
第八共同発明者の署名	日付	Eighth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第九共同発明者名		Full name of ninth joint inventor, if any	
第九共同発明者の署名	日付	Ninth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第十共同発明者名		Full name of tenth joint inventor, if any	
第十共同発明者の署名	日付	Tenth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	